ABSTRACT

According to an aspect of the present invention, there is provided a simulation circuit pattern evaluation method including: designing an aggregate of simulation circuit patterns, which simulate a circuit pattern of a semiconductor integrated circuit, by combining plural geometrical structure defining parameters respectively having at least two states in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters; forming the aggregate of the simulation circuit patterns on a substrate; and evaluating the formed aggregate of the simulation circuit patterns.